UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/656,551	09/06/2000	Zheng Zhang	10991625-1	9625

22879 7590 03/05/2004

HEWLETT PACKARD COMPANY
P O BOX 272400, 3404 E. HARMONY ROAD
INTELLECTUAL PROPERTY ADMINISTRATION
FORT COLLINS, CO 80527-2400

EXAMINER	
PUENTE, EMERSON C	
ART UNIT	**PAPER NUMBER**
2113	12

DATE MAILED: 03/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/656,551	Applicant(s) ZHANG ET AL.	
	Examiner Emerson C Puente	Art Unit 2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 February 2004* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☐ Claim(s) _____ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *7-9* is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claims 1-9 have been examined.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. § 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 2, and 4 are rejected under 35 U.S.C. § **103(a)** as being unpatentable over US Patent No. 6,079,030 of Masubuchi in view of US Patent No. 6,292,880 of Mattis et al. referred hereinafter "Mattis".

In regards to claim 1, Masubuchi discloses a computer system comprising:

an application memory organized as a plurality of cache lines, each cache line being identified by an address (see figure 10 item 26 and figure 1-3 item 32 and column 1 line 56-57 and column 3 lines 20-25 and column 6 lines 40-49);

a buffer for storing a plurality of cache lines (see figure 10 item 28 and figure 1-3 item 33 and column 1 lines 49-53).

a central processing unit (CPU) for executing instructions stored in said application memory (see figure 10 item 10 and figure 1-3 item 30 and column 1 lines 56-57 and column 2 lines 35-36);

a state memory for storing the contents of the internal registers of said CPU (see column 2 lines 55-58);

a checkpoint controller for defining a series of repeating checkpoint cycles, said checkpoint controller having access to a plurality of registers in said CPU that defines the state of that CPU at a point in each of said checkpoint cycles that is controllable by said checkpoint controller(see column 2 lines 13-24); and

a memory controller for operating said application memory and said buffer, said memory controller receiving a cache line from said CPU in response to a write command specifying an address A in said application memory at which said cache line is to be stored, wherein a copy of said cache line as stored in said application memory at address A, is copied into said buffer upon receiving the first write command specifying A after the start of the current checkpoint cycle, said cache line received in said write command replacing the contents of A in said application memory (see column 1 lines 59-65).

However, Masubuchi fails to disclose:

receiving the first write command specifying A after the start of the current checkpoint cycle but not on a subsequent write command specifying A during said current checkpoint cycle

Mattis discloses storing only one copy of data in cache (see abstract), indicating receiving the first write command specifying A after the start of the current checkpoint cycle but not on a subsequent write command specifying A during said current checkpoint cycle.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Masubuchi to receive the first write command specifying A after the start of the current checkpoint cycle but not on a subsequent write command specifying A during said current checkpoint cycle. A person of ordinary skill in the art would have been motivated to make the modification to Masubuchii because storing only one copy enables the storage usage to be dramatically reduced, as per teaching of Mattis (see abstract).

In regards to claim 2, Masubuchi discloses a computer system wherein each checkpoint cycle comprises a computational phase and a checkpoint phase. Masubuchi discloses write processing from the processor, indicating a computational phase (see column 1 lines 59-60) and further discloses the act of storing the contents of the main memory and the internal state of the processor, indicating a checkpoint phase (see column 2 lines 12-24);

and wherein said checkpoint controller during said checkpoint phase causes said CPU to write back to said application memory all dirty cache lines and to store internal registers defining the state of said CPU in said state memory. Masubuchi discloses at the time of a checkpoint the internal states of the processor, which constitute as internal registered defining the state of said CPU in said memory and the updated data item held in the cache, which constitute dirty cache lines, are written back to memory (see column 3 lines 20-25).

In regards to claim 4, Masubuchi discloses a computer system wherein said checkpoint controller, in response to a determination that a processing error has occurred, copies the contents of said buffer into said application memory, causes said CPU to copy the contents of said state memory into said CPU's internal registers, and restarts said computer system. Masubuchi discloses to bring the main memory into the preceding state, the memory control section reads and writes the data from the before image buffer (see column 2 lines 4-8), indicating copies the contents of said buffer into said application memory. He further states performing a checkpoint at suitable time intervals and storing the internal states of all of the processors, it is possible to return control from any point in time to the checkpoint (see column 2 lines 55-58), indicating copying contents of state memory into said CPU's internal registers and restarting said computer to the checkpoint.

Claim 3 is rejected under 35 U.S.C. § **103(a)** as being unpatentable over Masubuchi in view of Mattis and in further view of Applicant's Admitted Prior Art, referred hereinafter "AAPA"

In regards to claim 3, Masubuchi fails to disclose wherein the checkpoint controller empties the contents of the buffer at the end of the checkpoint phase if no error has been detected by the end of the checkpoint phase.

However, AAPA discloses wherein the checkpoint controller empties the contents of the buffer at the end of the checkpoint phase if no error has been detected by the end of the checkpoint phase (see page 2 lines 1-10).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Masubuchi to empty the contents of the buffer at the end of the checkpoint phase if no error has been detected by the end of the checkpoint phase because upon determination at the end of the checkpoint phase there is no error, it is determined that the contents in the memory are valid, and thus, there is no need of the information of the buffer. By emptying the contents of the buffer, one is able to free up space for the next cycle.

Claims 5-6 are rejected under 35 U.S.C. § **103(a)** as being unpatentable over Masubuchi in view of AAPA and Mattis.

In regards to claim 5, Masubuchi discloses a computer system comprising:

an application memory organized as a plurality of cache lines, each cache line being identified by an address (see figure 10 item 26 and figure 1-3 item 32 and column 1 line 56-57 and column 3 lines 20-25 and column 6 lines 40-49);

a buffer for storing a plurality of cache lines (see figure 10 item 28 and figure 1-3 item 33 and column 1 lines 49-53).

a central processing unit (CPU) for executing instructions stored in said application memory (see figure 10 item 10 and figure 1-3 item 30 and column 1 lines 56-57 and column 2 lines 35-36);

a state memory for storing the contents of the internal registers of said CPU (see column 2 lines 55-58);

a checkpoint controller for defining a series of repeating checkpoint cycles, said checkpoint controller having access to a plurality of registers in said CPU that defines the state of that CPU at a point in each of said checkpoint cycles that is controllable by said checkpoint controller(see column 2 lines 13-24); and

a memory controller for operating said application memory and said buffer, said memory controller receiving a cache line from said CPU in response to a write command specifying an address A in said application memory at which said cache line is to be stored, wherein a copy of said cache line as stored in said application memory at address A, is copied into said buffer upon receiving the first write command specifying A after the start of the current checkpoint cycle, said cache line received in said write command replacing the contents of A in said application memory in response a determination that a processing error has occurred, copies the contents of said buffer into said application memory, causes said CPU to copy the contents of said memory into said CPU's internal registers, and restart said computer system (see column 1 lines 59-65) , and.

wherein said checkpoint controller causing said computer system to be reconfigured before restarting said computer system (see column 1 lines 15-22).

However, Masubuchi fails to disclose:

a FIFO buffer.

receiving the first write command specifying A after the start of the current checkpoint cycle but not on a subsequent write command specifying A during said current checkpoint cycle

AAPA disclose:

a computer system that uses a FIFO buffer to reconstruct the state of a slave computer's memory to the last checkpoint (see page 1 lines 27-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Masubuchi to use a FIFO buffer. A person of ordinary skill in the art would have been motivated to make the modification to Masubuchi because Masubuchi disclose a buffer for retaining the preceding state of the memory and a FIFO buffer, as per teaching of AAPA, constitutes a buffer, which can be used to retain the preceding state of the memory.

Furthermore, Mattis discloses storing only one copy of data in cache (see abstract), indicating receiving the first write command specifying A after the start of the current checkpoint cycle but not on a subsequent write command specifying A during said current checkpoint cycle.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Masubuchi to receive the first write command specifying A after the start of the current checkpoint cycle but not on a subsequent write command specifying A during said current checkpoint cycle. A person of ordinary skill in the art would have been motivated to make the modification to Masubuchii because storing only one copy enables the storage usage to be dramatically reduced, as per teaching of Mattis (see abstract).

In regards to claim 6, Masubuchi discloses a computer system comprising:

an application memory organized as a plurality of cache lines, each cache line being identified by an address (see figure 10 item 26 and figure 1-3 item 32 and column 1 line 56-57 and column 3 lines 20-25 and column 6 lines 40-49);

a buffer for storing a plurality of cache lines (see figure 10 item 28 and figure 1-3 item 33 and column 1 lines 49-53).

a central processing unit (CPU) for executing instructions stored in said application memory (see figure 10 item 10 and figure 1-3 item 30 and column 1 lines 56-57 and column 2 lines 35-36);

a state memory for storing the contents of the internal registers of said CPU (see column 2 lines 55-58);

a checkpoint controller for defining a series of repeating checkpoint cycles, said checkpoint controller having access to a plurality of registers in said CPU that defines the state of that CPU at a point in each of said checkpoint cycles that is controllable by said checkpoint controller(see column 2 lines 13-24); and

a memory controller for operating said application memory and said buffer, said memory controller receiving a cache line from said CPU in response to a write command specifying an address A in said application memory at which said cache line is to be stored, wherein a copy of said cache line as stored in said application memory at address A, is copied into said buffer upon receiving the first write command specifying A after the start of the current checkpoint cycle, said cache line received in said write command replacing the contents of A in said application memory (see column 1 lines 59-65).

a computer system wherein said application memory comprises fault tolerant memory. Masubuchi disclose the buffer memory for retaining the preceding state of the memory, indicating a fault tolerant memory (see figure 10 item 28 and figure 1-3 item 33 and column 1 lines 49-53).

However, Masubuchi fails to disclose

a FIFO buffer.

receiving the first write command specifying A after the start of the current checkpoint cycle but not on a subsequent write command specifying A during said current checkpoint cycle

AAPA disclose:

a computer system that uses a FIFO buffer to reconstruct the state of a slave computer's memory to the last checkpoint (see page 1 lines 27-30).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Masubuchi to use a FIFO buffer. A person of ordinary skill in the art would have been motivated to make the modification to Masubuchi because Masubuchi

disclose a buffer for retaining the preceding state of the memory and a FIFO buffer, as per teaching of AAPA, constitutes a buffer, which can be used to retain the preceding state of the memory.

Furthermore, Mattis discloses storing only one copy of data in cache (see abstract), indicating receiving the first write command specifying A after the start of the current checkpoint cycle but not on a subsequent write command specifying A during said current checkpoint cycle.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teaching of Masubuchi to receive the first write command specifying A after the start of the current checkpoint cycle but not on a subsequent write command specifying A during said current checkpoint cycle. A person of ordinary skill in the art would have been motivated to make the modification to Masubuchii because storing only one copy enables the storage usage to be dramatically reduced, as per teaching of Mattis (see abstract).

Response to Arguments

Applicant's arguments filed December 5, 2003 have been fully considered but they are not deemed to be persuasive.

In response regarding claim 1,5, and 6 to applicant's argument that states on page 11, "In accordance with the exemplary embodiments, a copy of a cache line is only stored the first time that the cache line is written during a current checkpoint cycle. As such, a much smaller buffer memory can be used, since copies of the cache line are not stored on subsequent writes to the same address of the buffer during the current checkpoint cycle" and on page 13, "Mattis patent does not teach or suggest configuring a cache as a FIFO buffer which receives a first write command specifying an address A after a start of the current checkpoint cycle, but not on a subsequent write command specifying A during said current checkpoint cycle. In addition, there would be no motivation to have used features of the Mattis patent in conjunction with the Masubuchi patent," examiner respectfully disagrees. Mattis teaches detecting duplicate objects and storing only one copy of the duplicate object (see abstract), indicating a copy is only stored the first time that it is written. If Masubuchi, which discloses receiving a first write command specifying an address A after a start of the current checkpoint cycle, were to detect for duplicates

and stores only one copy of the duplicate, as per teachings of Mattis, then a copy of a cache line is only stored the first time that the cache line is written during a current checkpoint cycle, thus indicating receiving a first write command specifying an address A after a start of the current checkpoint cycle, but not on a subsequent write command specifying A during said current checkpoint cycle.

Examiner maintains his rejection.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, one would be motivated to make the modification to Masubuchii because storing only one copy enables the storage usage to be dramatically reduced, as per teaching of Mattis (see abstract). Examiner maintains his rejection.

In response regarding claim 5 on page 16 to applicant's request regarding that the Examiner provide some teaching in the prior art which forms the basis for the assertion of Official Notice other that Applicant's own description of exemplary embodiments, examiner has withdrawn official notice and rejected the limitation based on Masubuchi reference column 1 lines 10-15 which cites "After having executed a program and finished the process, ordinary computers generally cannot return control to the preceding state and then restart the process. In the following various application techniques, however, it is desirable to use the function of returning the contents of the memory to the preceding state and resuming the process at that point in time (the memory state recovering function)", thus indicating reconfiguring before restarting said computer system. Thus, argument is moot.

Allowable Subject Matter

Claims 7-9 are allowable over the prior art of records as indicated in the previous office action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Emerson C Puente whose telephone number is (703) 305-8012. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W Beausoliel can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-5631.

Emerson Puente
3/2/04

ROBERT BEAUSOLIEL
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100